Concurrent Multiband Low-Noise Amplifiers—Theory, Design, and Applications

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Invited Paper

***Abstract*—The concept of *concurrent* multiband low-noise-amplifiers (LNAs) is introduced. A systematic way to design concurrent multiband integrated LNAs in general is developed. Applications of concurrent multiband LNAs in concurrent multiband receivers together with receiver architecture are discussed. Experimental results of a dual-band LNA implemented in a 0.35-μm CMOS technology as a demonstration of the concept and theory is presented.**

***Index Terms*—Amplifier noise, land mobile radio cellular systems, low-noise amplifier, radio communication, radio receivers.**

I. Introduction

STANDARD receiver architectures, such as superheterodyne and direct conversion, accomplish high selectivity and sensitivity by narrow-band operation at a single input frequency [1]. These modes of operation limit the system's available bandwidth and robustness to channel variations and thus its functionality. On the other hand, wide-band modes of operation are more sensitive to out-of-band unwanted signals (blockers) due to transistor nonlinearity. These out-of-band blockers can severely degrade receiver's sensitivity.

The diverse range of modern wireless applications necessitates communication systems with more bandwidth and flexibility. More recently, dual-band transceivers have been introduced to increase the functionality of such communication systems by switching between two different bands to receive *one band at a time* [2]–[5]. While switching between bands improves the receiver's versatility (e.g., in multiband cellular phones), it is not sufficient in the case of a multifunctionality transceiver where more than one band needs to be received simultaneously (e.g., a multiband cellular phone with a global positioning system, global position system (GPS), receiver and a Bluetooth interface). Using conventional receiver architectures, simultaneous operation at different frequency bands can only be achieved by building multiple independent signal paths with an inevitable increase in the cost, footprint, and power dissipation. Although there have been efforts to minimize the number of additional components used for the second band of operation (e.g., for adding GPS to a CDMA phone [6]), none of these efforts attempt simultaneous reception of more than one band.

In this work, a new *concurrent* dual-band receiver architecture is introduced that is capable of simultaneous operation at two-different frequencies without dissipating twice as much power or a significant increase in cost and footprint [7]. This concurrent operation can be used to extend the available bandwidth, provide new functionality, and/or add diversity to battle channel fading. The concurrent operation is realized through an elaborate frequency conversion scheme in conjunction with a novel concurrent dual-band low-noise amplifier (LNA). These new concurrent multiband LNAs provide simultaneous narrow-band input matching and gain at multiple frequency bands, while maintaining low noise.

Section II reviews the current advances of single-band LNAs from technological and architectural points of view. Section III briefly describes one such receiver architecture demonstrating the central role of the concurrent LNAs in the receiver. The general design methodology of concurrent multiband LNAs is discussed in Section IV. Experimental results of a concurrent dual-band CMOS LNA will be presented in Section V.

II. A Review of Single-Band LNA Design Issues

Being the first active element in the receiver chain, the noise figure (NF) of an LNA plays a significant role in the overall NF of the receiver, which controls its sensitivity and output signal-to-noise ratio (SNR) [8]. Before exploring the design details of concurrent multiband LNAs, it is helpful to review some of the existing technological and topological choices for single-band LNAs.

A. Technology

The bipolar junction transistor was the first solid-state active device to provide practical gain and NF at microwave frequencies [9]. In the seventies, breakthroughs in the development of field-effect transistors (FETs) (e.g., GaAs MESFET) led to higher gain and lower NF than bipolar transistors for the frequencies in the range of several gigahertz [10]. Currently, advanced FETs and bipolar transistors still compete for lower NF and higher gain at frequencies in excess of 100 GHz.

Manuscript received May 28, 2001. This work was supported by Conexant Systems and by NSF-ERC.

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Publisher Item Identifier S 0018-9480(02)00843-8.

Examples are the high electron-mobility transistors (HEMTs), such as pseudomorphic high electron-mobility transistors (pHEMTs) [11], metamorphic high electron-mobility transistors (MHEMTs) [12], as well as heterojunction bipolar transistors (HBTs) [13], [14], built using a variety of semiconductor materials (e.g., GaAs, InP, Si, SiGe).

Traditionally, very low-noise amplifiers at high frequencies have been made using transistors with high electron mobility and high saturation velocity on high-resistivity substrates for the following principal reasons.

1) Higher carrier mobility and peak drift velocity result in a higher transistor transconductance and shorter carrier transit time [10] for a given current, thus allowing for the reduction of the dc current for the same transconductance (gain) in transistors which lowers the input-referred noise and, hence, the NF. This gives compound semiconductors a significant advantage over silicon, as for instance, the electron mobility and the peak drift velocity are typically six and two times larger, respectively, for GaAs when compared to silicon [10].
2) Higher carrier mobility also results in lower parasitic drain and source series resistors. The parasitic source resistance can be a major contributor to the overall NF of certain LNAs, such as those used for satellite communications.
3) Due to mostly technological limitations, the series input resistance of silicon-based transistors is usually higher than those of compound semiconductors. In particular, the lower resistance of the metal gate of GaAs MESFETs compared to higher resistance of the poly-silicon gate in MOSFETs and thin bases in bipolar transistors, result in a lower NF for GaAs transistors.
4) The loss properties of on-chip passive components can have a significant effect on the noise and gain performance of the LNAs. High-resistivity substrates minimize the substrate loss components. As the loss and noise are closely related through the fluctuation-dissipation theorem of statistical physics [15], [16], the energy loss reduction translates to a lower NF for the amplifier.

Despite the above mentioned limitations of silicon technologies, several silicon LNAs have been reported. Meyer *et al.* reported one of the early LNAs made on a low-resistivity (i.e., lossy) silicon substrate using bipolar junction transistors for commercial cellular applications [17], where very low NF is not needed. Recently, a large number of efforts have been reported to use the advanced digital CMOS processes for single-chip implementation of the complete radio transceiver [18], [19]. Significant progress in CMOS LNA design has been made during the last several years where more recent results, such as [20], demonstrate significant improvements over the earlier works [21]–[23] and show that CMOS LNAs can be a worthy competitor for compound semiconductor implementations in many portable applications.

B. Topology

Although several different topologies have been proposed to implement LNAs, we will only focus on two most common single-stage[1] LNAs in CMOS processes, namely, the common-gate topology [22] and inductively degenerated common-source stage [23], [24], shown in Fig. 1.

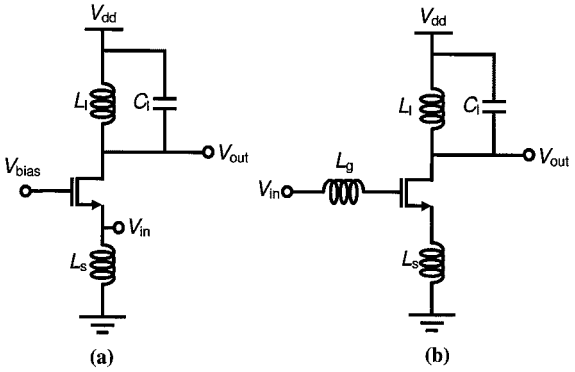

Fig. 1. Commonly used single-band CMOS LNAs. (a) Common-gate. (b) Common-source with inductive degeneration.

The common-gate configuration uses the resistive part looking into the source of the transistor to match the input to a well-defined source impedance (e.g., 50 Ω). This impedance is $1/(g_m + g_{mb})$ in the case of a MOSFET, where g_m and g_{mb} are transconductances of the top-gate and back-gate transistors, respectively. However, it can be shown that the NF is lower bounded to 2.2 dB for a perfectly matched long-channel CMOS transistor [22] unless a transformer is used at the input [25].

In a common-source LNA, inductive degeneration is used to generate the real part needed to match the LNA input to the preceding antenna or filter. Strutt and Van der Ziel first noticed that inductive degeneration can enhance the output SNR [26]. The ideal lossless inductive feedback moves the source impedance for optimum NF toward the optimum power match with a minor increase in the minimum NF [27]. Unfortunately, in silicon implementations, the loss associated with inductors will degrade the NF. It should be mentioned that in these cases cascode configuration can be used to enhance the stability and reverse-isolation of the amplifier.

While the problem of achieving the lowest noise in an amplifier has been solved for a general case through a mathematical treatment [28], this general approach still does not provide the necessary insights into the design.

An alternative approach is to use Smith charts to find the optimum impedance for noise and power matching at the input of the amplifier for given active device [29]–[31]. Although the Smith chart is a very convenient tool for seeing how close we are to the minimum NF and the maximum gain of a given device, it does not show the effect of individual noise sources on the total NF. This is particularly important for a concurrent multiband LNA, since different noise sources behave differently at different frequencies.

Unlike bipolar transistors whose dc current sets the transconductance and minimum noise-figure, MOSFETs offer extra degrees of freedom in choosing the device width and length. These extra degrees of freedom can be used to improve the NF and the gain of the amplifier. Recently, some work has been done to calculate and minimize the NF of a single-band common-source

[1]This discussion is also valid for the first stage of multistage LNAs.

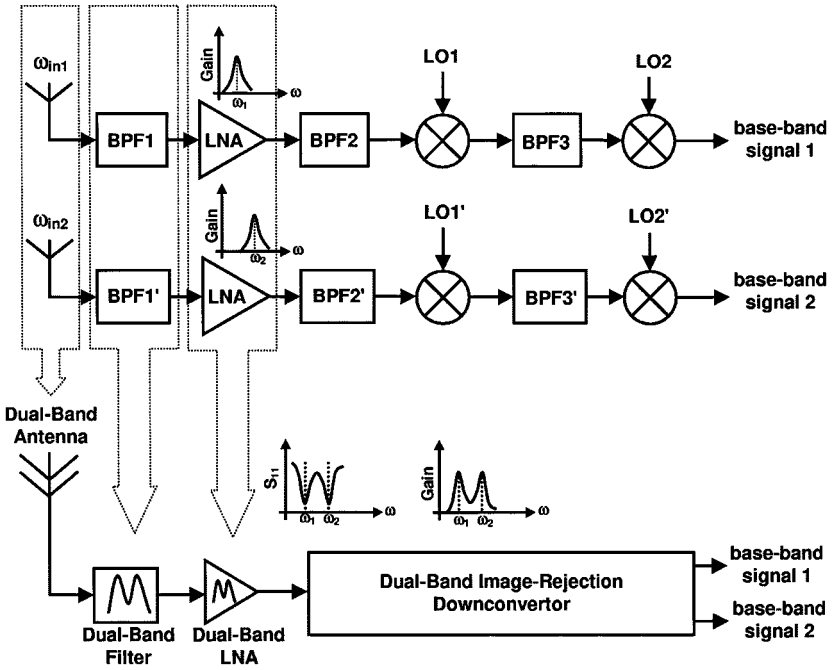

Fig. 2. Evolution process of two parallel receivers to a concurrent dual-band receiver.

CMOS LNA with inductive degeneration using a more systematic approach [23]. In the next section, we will introduce the concept of a concurrent receiver and a new architecture to implement it. In Section IV, we present a general approach for the design of concurrent multiband LNAs which are important building blocks in concurrent receivers.

III. Concurrent Receiver Architectures

In this section, we will develop a concurrent dual-band receiver architecture that can be fully integrated. The objective is to devise a receiver that can simultaneously receive signals at two different frequency bands with maximum reuse of power and building blocks.

Fig. 2 shows the conceptual evolution of a dual-band receiver, starting with two totally independent heterodyne receiving paths, and leading to an efficient concurrent dual-band receiver.

The first gain stage in a concurrent dual-band receiver is its LNA. Traditional single-band LNAs use a single or cascode transistor stage to provide wide-band transconductance and combine it with proper passive resonant circuitry at the input and output as discussed briefly in the previous section. This approach shapes the frequency response, ensures stability, and achieves gain and matching at the single band of interest [31].

A very important observation is that the transconductance of the transistor is inherently wide-band and can be used to provide gain and matching at other frequencies without any penalty in the power dissipation. This observation leads to a compact and efficient front-end for a concurrent dual-band receiver which consists of a dual-band antenna [32]–[34], followed by a monolithic dual-band filter [35] and a concurrent dual-band LNA that provides simultaneous gain and matching at two bands, as shown at the bottom of Fig. 2. A detailed approach to the design of such a multiband LNA will be described in the subsequent sections. It should be noted that the concurrent dual-band

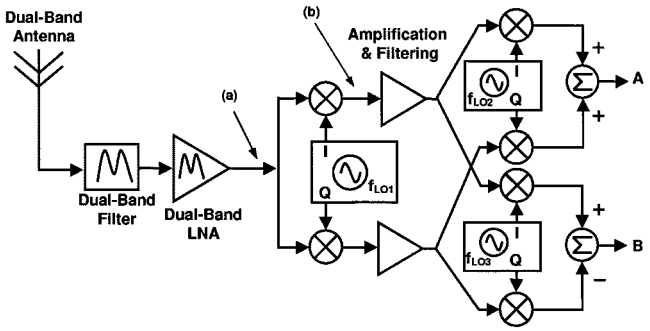

Fig. 3. An architecture for concurrent dual-band receiver.

receiver does not need any dual-band switch [36] or diplexer [37], because simultaneous reception at both bands is desired. Then a dual-band down-conversion scheme is needed to translate different information carrying signals to baseband with as few local oscillators (LOs) and external filters as possible, while maintaining isolation between the two bands. This can be done in many different ways, for instance, Fig. 3 shows a simplified block diagram of one such receiver.

The frequency of the first LO that appears after the LNA and performs the first down conversion determines the image frequency(ies) and plays an important role in the performance of the system. For a *nonconcurrent* receiver, it has been proposed to choose the first LO frequency halfway between the two frequency bands and select the band of interest by choosing the appropriate sideband produced by an image-separation mixer [2]. Although this method is sufficient for the nonconcurrent approaches, it will suffer from some serious shortcomings if used for a *concurrent* receiver, where the LNA amplifies the signal in both of the desired bands. This is because one band is the image of the other and there is no attenuation of the image by either the antenna or the filter. The situation is exacerbated by the LNA

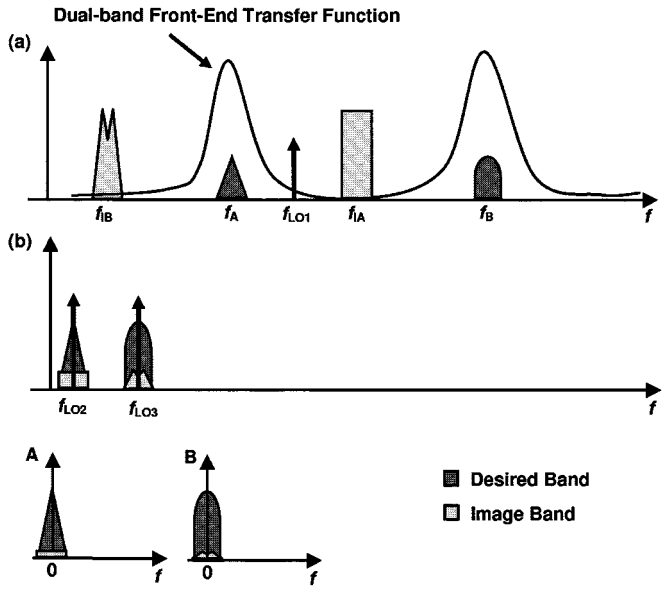

Fig. 4. Frequency-domain signal evolution in the concurrent dual-band receiver of Fig. 3.

gain in the image band. In this scenario, one is solely relying on the image rejection of the single sideband receiver, which is limited by the phase and amplitude mismatch of the quadrature LOs and the signal paths [38], [39], and is insufficient in a concurrent receiver.

An alternative approach that does not suffer from the above problem and, in fact, significantly improves the image rejection is to use an offset LO as shown in Fig. 4. The LO frequency is offset from the midpoint of the two bands of interest (f_A and f_B) in such a way that the image of the first band at f_A falls at the notch of the front-end transfer function at f_{IA}. The attenuation at f_{IA} is determined by the compounded attenuation of the dual-band antenna, filter, and LNA. Similarly, the image of the second band at f_B will fall outside the passband of the front-end at f_{IB} and will be attenuated, accordingly. Using a quadrature first LO makes the stage fit to act as the first half of any single-sideband image-reject architecture, such as that proposed by Weaver [40]. Since the receiver has to demodulate two bands concurrently and independently, two separate paths *must* be used eventually. Each path comprises the second half of the image reject architecture, as shown in Fig. 3, which provides further image rejection (Fig. 4). This architecture eliminates an extra antenna, a front-end filter, an LNA, and a pair of high-frequency mixers, which in turn results in power, footprint, and area savings. At the same time, large image rejection in excess of that of the single-sideband receiver is achieved through diligent frequency planning and proper usage of stop-band attenuation.

IV. Concurrent Multiband LNA

In a single-band LNA, passive networks are used to shape the response of the wide-band transconductance of the active device in the frequency domain to achieve gain and matching at the frequency of interest. This concept can be generalized to multiple frequency bands noting that the intrinsic transconductance of the active device is inherently wide-band and can be used at multiple frequencies simultaneously.

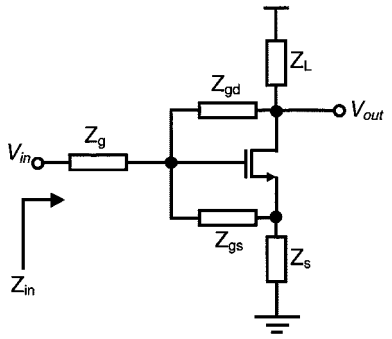

Fig. 5. General model for a single-stage amplifier in common-source configuration.

It is crucial to note the fundamental differences between the concurrent and the existing nonconcurrent approaches. In conventional dual-band LNAs, either one of the two single-band LNAs is selected according to the instantaneous band of operation [41], [42], or two (three) single-band LNAs are designed to work in parallel using two (three) separate input matching circuits and two (three) separate resonant loads [2], [43]. The former approach is nonconcurrent, while the latter consumes twice (three times) as much power if used in a concurrent setting. The other existing approach is to use a wide-band amplifier in the front-end [44]. Unfortunately, in a wide-band LNA, strong unwanted blockers are amplified together with the desired frequency bands and significantly degrade the receiver sensitivity.

In this section, we present an analytical approach to the design of a general class of integrated concurrent multiband LNAs. The concurrent LNA is proposed as a solution to the aforementioned problems in a concurrent receiver.

A. General Amplifier in Common-Source Configuration

In this section, we use a general model for an amplifier in the common-source configuration to obtain an equivalent circuit for the input impedance and a general expression for the gain at multiple frequencies. This equivalent circuit will be used to achieve simultaneous power and noise matching in a concurrent multiband LNA. Fig. 5 shows a transistor[2] with arbitrary gate impedance Z_g, gate–source impedance $Z_{\rm gs}$, source impedance Z_s, gate–drain impedance $Z_{\rm gd}$, and load impedance Z_L. The impedances shown in Fig. 5 also include the transistor's inherent passive components (e.g., $C_{\rm gs}$, $C_{\rm gd}$). General expressions for input impedance and voltage-gain of this amplifier are found in Appendix A.

B. Input Matching

The input of the LNA is either fed directly by the antenna or is connected to the antenna through a bandpass filter, a diplexer/duplexer, or both. In any case, the impedance looking into the input of the LNA should be power matched (i.e., complex conjugate matched)[3] to the impedance of the preceding stage for maximum signal power transfer. Additionally, it is

[2]While the general active device discussed here is a MOS transistor, a similar analysis applies to other active devices (e.g., BJT, MESFET.)

[3]In large-signal devices, power match does not necessarily correspond to the complex conjugate matching. However, since the LNA design is based on small-signal principals, we can use two terms, synonymously.

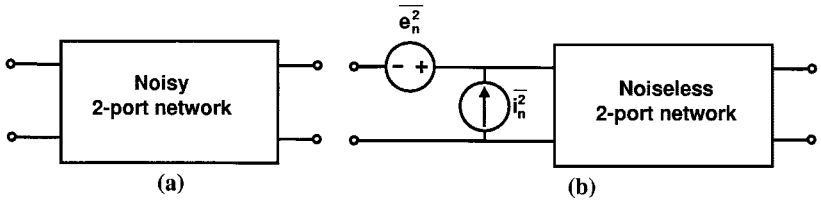

Fig. 6. General representation of any (a) noisy two-port and (b) its equivalent circuit.

essential to provide the correct impedance to the preceding stage to satisfy its nominal specifications (e.g., bandpass filter characteristics, such as rolloff, etc., depend on filter loading).

The expressions in Appendix A can be further simplified if we assume that $Z_{\rm gd}$ is much larger than the other impedances. This assumption neglects the effect of the transistor's intrinsic $C_{\rm gd}$ and its associated Miller effect. Then, the input impedance expression of (21) simplifies to

$$Z_{\rm in} = Z_g + Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs}). \tag{1}$$

This expression will be used in the following section to design multiband input matching networks.

Theoretically, the input impedance of any stable amplifier with a nonzero real part can be perfectly matched to any arbitrary source impedance (with a positive real part) for a single frequency using lossless passive components at the input of the amplifier [45]. Equation (1) can be used to generalize this *power match* concept to multiple frequencies. It can be used to generate numerous topologies to achieve simultaneous impedance matching at multiple distinct frequencies.

In an LNA, it is also necessary to achieve a *noise match* at the input for the frequency(ies) of interest to minimize the NF. In the following section on noise matching, we will demonstrate that one way to minimize the NF of the amplifier of Fig. 5 is by designing the passive network so that it satisfies $Z_g + Z_{\rm gs} + Z_s' = 0$ at multiple frequencies of interest. However, this can only be achieved using lossless passive components. Therefore, in practice, one should minimize $Z_g + Z_{\rm gs} + Z_s'$, to its smallest real part, $R_{\rm min}$. Having satisfied the above condition, the input impedance will be

$$Z_{\rm in} = g_m Z_{\rm gs} Z_s' + R_{\rm min}. \tag{2}$$

Theoretically, a large number of passive topologies for $Z_{\rm gs}$ and Z_s' can provide input impedance matching at multiple frequency bands. One particular example which is of great practical value is when $Z_{\rm gs}$ is just the intrinsic gate–source capacitance, $C_{\rm gs}$ and, hence, Z_s' has to be an inductor as in the single-band common-source LNA in [26], [24], [23]. For negligible passive loss ($R_{\rm min} \approx 0$) and a real-value impedance $Z_{\rm in}$, $R_{\rm in}$ (e.g., 50 Ω for most practical cases), the source inductor is given by

$$L_s = \frac{R_{\rm in} C_{\rm gs}}{g_m} \approx \frac{R_{\rm in}}{\omega_T}. \tag{3}$$

This will result in a passive network for Z_g that will minimize $Z_g + Z_{\rm gs} + Z_s'$ for all the frequencies of interest. One example of such a design can be found in Section V.

The optimum source inductance depends on ω_T and, hence, process parameters, as (3) suggests. Ignoring $C_{\rm gd}$, in a deep short-channel CMOS biased in the velocity saturation region, ω_T is approximately given by

$$\omega_T \cong \frac{g_m}{C_{\rm gs}} = \frac{3}{4}\mu_n \frac{E_C}{L} = \frac{3}{4} \cdot \frac{v_{\rm sat}}{L} \tag{4}$$

where μ_n is electron mobility in the channel, E_C is the critical field, $v_{\rm sat}$ is the saturation velocity, and L is transistor's channel length. Therefore, for a given deep submicrometer CMOS technology with constant channel length where carriers are velocity saturated, the value of L_s is almost fixed and is independent of the bias current and the device size. For a bipolar transistor, ω_T has a current dependency. However, if junction capacitors are negligible for a transistor biased with a high collector current, this current dependency is small and again the value of L_s is independent of bias current. In a long-channel CMOS, ω_T depends on the bias current and the device width and so will L_s.

C. Noise Matching

An important design parameter in receiver design, which is the measure of receiver noise, is the noise factor F (also known as NF, when expressed in decibels). The definition of the noise factor of any transducer (e.g., LNA, mixer, filter, etc.) given by [46] is

$$F = \frac{N_{\rm total}}{N_{\rm source}} \tag{5}$$

where $N_{\rm total}$ is the total noise power per unit bandwidth available at the output port[4] at a corresponding output frequency when the noise temperature of its input termination is a standard 290 K at all frequencies and $N_{\rm source}$ is that portion of $N_{\rm total}$ engendered at the input frequency by the input termination at the standard noise temperature[5] 290 K.

Any noisy two-port network can be represented by a noiseless two-port network with input equivalent voltage e_n and current

[4]Actually, noises can be referred to any other node, e.g., input node, in the circuit.

[5]While the NF is a useful parameter in practice, it is an incomplete measure of an LNA's performance, as it is desirable to have a low NF *while* maintaining a high gain. For example, feedback can be used to reduce F as close to unity as possible, at the price of lowering the gain in the process [28], [47]. Cascading multiple stages of such feedback amplifiers to recover the original gain will result in a noise factor larger than or equal to the noise factor of the original amplifier without feedback [48]. A more accurate measure of an amplifiers noise performance, called the noise measure M is defined in [28] to take the effects of both gain and NF into account.

sources i_n, [49], as shown in Fig. 6. Then, the noise-factor F will be given by

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s e_n|^2}}{\overline{i_s^2}} \tag{6}$$

where Y_s is the reference source admittance (e.g., $Y_s = 1/50\ \Omega$) for the NF and i_s is the noise current associated with it.

In general, equivalent input voltage and current sources are correlated. The effect of adding components in series or parallel to the input of the network on the equivalent input voltage and current noise sources can be easily modeled by the *noise-source transformations* (Appendix B).

Now, we will find an expression for the NF of the general single-stage common-source amplifier of Fig. 5. While it is possible to include all the different noise sources in the calculations, we will make certain simplifying assumptions to keep the expressions tractable. In the following calculations, we assume that the only dominant noise sources are the drain and gate-induced current source i_{nd} and i_{ng} [50] for the MOS transistor and collector and base shot noise currents i_{nc} and i_{nb} for the bipolar transistor. It is also assumed that passive impedances shown in Fig. 5 do not contribute any noise. The noise of any physical input resistance r_g at the input appears as an additional term r_g/R_s in the expressions for F. Practically, r_g and r_b are very important in determining the NF, as well as input impedance of the LNA. They determine the minimum noise-factor ($F_{\min}$) of a transistor [29].

Using these simplifying assumption, the equivalent input current and voltage sources for the amplifier in Fig. 5 are

$$\begin{cases} i_n = \alpha_{nd} \cdot i_{nd} + \alpha_{ng} \cdot i_{ng} \\ e_n = Z_{nd} \cdot i_{nd} + Z_{ng} \cdot i_{ng} \end{cases} \tag{7}$$

where

$$\begin{aligned} \alpha_{ng} &= \frac{Z_{\rm gs}(1 - g_m Z_{\rm gd})}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs}) - g_m Z_{\rm gs} Z_{\rm gd}} \\ \alpha_{nd} &= -\frac{Z_{\rm gs} + Z_{\rm gd}}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs}) - g_m Z_{\rm gs} Z_{\rm gd}} \\ Z_{ng} &= -\frac{g_m Z_{\rm gs} Z_s' Z_{\rm gd}}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs}) - g_m Z_{\rm gs} Z_{\rm gd}} \\ Z_{nd} &= -\frac{Z_{\rm gd}(Z_{\rm gs} + Z_s')}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs}) - g_m Z_{\rm gs} Z_{\rm gd}} \end{aligned} \tag{8}$$

combining (6) and (7) results in the following expression for the noise factor F:

$$\begin{aligned} F = 1 + |\alpha_{nd} + Y_s Z_{nd}|^2 \cdot \frac{\overline{i_{nd}^2}}{\overline{i_s^2}} + |\alpha_{ng} + Y_s Z_{ng}|^2 \cdot \frac{\overline{i_{ng}^2}}{\overline{i_s^2}} \\ + \frac{2\,\mathrm{Re}\left\{(\alpha_{nd} + Y_s Z_{nd})(\alpha_{ng} + Y_s Z_{ng})^* \cdot \overline{i_{nd} i_{ng}^*}\right\}}{\overline{i_s^2}} \end{aligned} \tag{9}$$

where the second term is due to drain current noise, the third term is caused by gate-induced current noise, and the last term is the result of the correlation between the two noise sources (a similar correlation term exists between the collector and base shot noise of a bipolar transistor [50]).

Note that (9) is quite general and can be used for the design of broad-band, narrow-band, or concurrent multiband LNAs using any kind of transistor, as long as the small-signal noise model of the transistor is known. We will use this expression to compare the effect of various noise sources in different topologies.

In the case of a MOS transistor, noise current densities are known to be [50]

$$\begin{aligned} \overline{i_{nd}^2} &= 4kT\gamma\, g_{d0} \Delta f \\ \overline{i_{ng}^2} &= 4kT\delta\, g_g \Delta f \\ g_g &= \frac{\omega^2 C_{\rm gs}^2}{5 g_{d0}} \\ \overline{i_{nd} i_{ng}^*} &= c^* \cdot \sqrt{\overline{i_{nd}^2}} \sqrt{\overline{i_{ng}^2}} \end{aligned} \tag{10}$$

where c^* is the complex conjugate of the correlation coefficient between gate and drain noise currents.

We can simplify (8) if we ignore $Z_{\rm gd}$ (setting $Z_{\rm gd} = \infty$), assuming it is dominated by the small gate–drain capacitor $C_{\rm gd}$ (i.e., a high impedance compared to other impedances in the circuit at the frequency of interest). Also, we can use the noise transformation of (24) to include the effect of an arbitrary gate series impedance Z_g. Under these assumptions, the coefficients in (7) will become

$$\begin{aligned} \alpha_{nd} &= \frac{1}{g_m Z_{\rm gs}} \\ \alpha_{ng} &= 1 \\ Z_{nd} &= \frac{Z_g + Z_{\rm gs} + Z_s}{g_m Z_{\rm gs}} \\ Z_{ng} &= Z_g + Z_s \end{aligned} \tag{11}$$

which can be used in (9) to estimate the NF of the LNA.

To gain more design insight, for the time being let us focus on the effect of the drain current noise, which is often the most dominant noise source in the amplifier. In this case, the noise factor is given by

$$F = 1 + |1 + Y_s(Z_g + Z_{\rm gs} + Z_s')|^2 \cdot \frac{1}{g_m^2 |Z_{\rm gs}|^2} \cdot \frac{\overline{i_{nd}^2}}{\overline{i_s^2}}. \tag{12}$$

Since Z_g, $Z_{\rm gs}$, and Z_s' are assumed to be passive networks, and Y_s is a real admittance in all the practical cases (e.g., 1/50 Ω), the minimum value of the first term of the product above occurs when

$$Z_g + Z_{\rm gs} + Z_s' = 0 \qquad \forall\, \omega_i \tag{13}$$

for all frequency bands, ω_i. For this to be possible, all three passive networks should be lossless. Therefore, in practice, one should choose the passive networks Z_g, $Z_{\rm gs}$, and Z_s' to minimize $Z_g + Z_{\rm gs} + Z_s'$ at each center frequency of interest, ω_i. We will refer to this minimum real value at each center frequency as $R_{\min}(\omega_i)$. This is the same constraint that we referred to in the previous subsection on the input matching of concurrent LNAs.

The above-mentioned general constraint for a concurrent multiband LNA should also work in the more straightforward case of a single-band LNA. In this case, if $Z_{\rm gs}$ is simply the

gate–source capacitance, and if Z_g and Z_s' networks consist of single inductors, we can satisfy (13) by setting

$$(L_s + L_g)C_{\rm gs}\omega_0^2 = 1 \tag{14}$$

where ω_0 is the center frequency of interest in the single-band LNA. This is the same design equation used in [23].

In addition to the minimization of $Z_g + Z_{\rm gs} + Z_s'$ at *each* center frequency of interest, (12) suggests that using higher $Z_{\rm gs}$ and higher device g_m can lower the NF further. One simple way of obtaining a large $Z_{\rm gs}$ is to keep the $Z_{\rm gs}$ network as simple as the intrinsic gate–source capacitance $C_{\rm gs}$, i.e., using no explicit component between the gate and the source.

Different transistor technologies result in different noise performances. To compare different technologies, we can rewrite the NF expression of (12) as the following general expression valid for both MOS and bipolar transistors:

$$F = 1 + 2k_L\,\frac{IR_s}{V_{\rm char}}\left(\frac{\omega}{\omega_T}\right)^2$$
$$k_L = \left(1 + \frac{R_{\rm min}(\omega)}{R_s}\right)^2 \tag{15}$$

where ω_T is the small-signal unity frequency of the transistor[6] and I is the drain (or collector) current. The characteristic voltage, $V_{\rm char}$, is defined as $V_{\rm char} = 4kT/q$ for a bipolar transistor, and $V_{\rm char} = (V_{\rm gs} - V_T)/\gamma$ and $V_{\rm char} = E_C L/\gamma$ for a long-channel and short-channel velocity-saturated MOS transistor, respectively.

Keeping in mind that to arrive at (15) we ignored the effect of the gate-induced current noise (or base shot noise), as well as the gate (base) series resistance noise, we can use (15) to make an approximate comparison between the noise performance of bipolar and MOS transistors. It can be seen from (15) that NF decreases with increasing $V_{\rm char}$, assuming constant ω_T. Table I shows the values of $V_{\rm char}$ and ω_T for a bipolar junction transistor as well as a few typical short-channel MOS transistors.[7] It is also noteworthy that, under these assumptions, a CMOS LNA will have a smaller NF compared to its bipolar counterpart because of its higher $V_{\rm char}$.[8] Nevertheless, this simplistic analysis is not completely adequate and, hence, a more accurate comparison will be performed next.

Taking the effect of the input resistance, gate-induced noise or base-shot noise into account, the following expression can be derived for the NF:

$$F_{\rm Bipolar} = 1 + \frac{r_b}{R_s} + 2k_L\,\frac{I_C R_s}{V_{\rm char}}\left(\frac{\omega}{\omega_T}\right)^2$$

[6]Note that ω_T is a fixed value for a given deep short-channel MOS transistor biased in velocity saturation region, but it depends on current and device width in a long-channel MOS transistor. ω_T is current-dependent in bipolar transistor, but the dependency is smaller for large collector currents and smaller junction capacitors.

[7]The E_C values in Table I are derived from curves of $g_m - V_{\rm gs}$ and $g_{d0} - V_{\rm gs}$ obtained from simulation using BSIM3v3 models and assuming $g_{d0}/g_m = 2(V_{\rm gs} - V_{th})/E_C L$ (i.e., deep velocity saturated device). Also we assume a γ of 2 and use (4) to obtain ω_T of MOS transistors.

[8]It should be noted that the same $V_{\rm char}$ appears in the phase-noise expressions of ring oscillators resulting in a similar argument suggesting that ring oscillators in current CMOS technologies offer lower phase noise than their bipolar counterparts [53].

TABLE I
COMPARISON OF $V_{\rm char}$, AND ω_T IN DIFFERENT SUBMICROMETER CMOS PROCESSES

Process technology	E_C (V/m)	$V_{\rm char}$ (V)	ω_T (rad/s)
Silicon Bipolar (τ_F = 3.67 ps)	N/A	0.140	2π × 37-GHz @ 10 mA
0.35-μm CMOS ($L_{\rm eff}$ = 0.27 μm)	5.46 × 10^6	0.74	2π × 42-GHz
0.25-μm CMOS ($L_{\rm eff}$ = 0.21 μm)	4.27 × 10^6	0.45	2π × 59-GHz
0.18-μm CMOS ($L_{\rm eff}$ = 0.16 μm)	3.02 × 10^6	0.24	2π × 63-GHz
0.15-μm CMOS ($L_{\rm eff}$ = 0.13 μm)	3.57 × 10^6	0.26	2π × 102-GHz

$$+\left(k_L + \frac{1}{\left(4\left(\frac{\omega}{\omega_T}\right)\cdot\frac{I_C R_s}{V_{\rm char}}\right)^2}\right)\cdot 2\,\frac{I_C R_s}{V_{\rm char}(\beta+1)} \tag{16a}$$

$$F_{\rm CMOS} = 1 + \frac{r_g}{R_s} + k_L\left(\frac{\omega C_{\rm gs}}{g_m}\right)^2\cdot\gamma g_{d0}R_s + \left(k_L + \left(\frac{1}{\omega C_{\rm gs}R_s}\right)^2\right)\cdot\delta\,\frac{\omega^2 C_{\rm gs}^2}{5g_{d0}}\,R_s + 2\sqrt{k_L}\,\frac{(\omega C_{\rm gs})^2}{g_m}\cdot|c|\cdot\sqrt{\frac{\gamma\delta}{5}}\cdot R_s. \tag{16b}$$

Note that no assumptions about the single-band operation of the amplifier were made and, hence, these equations are valid in the general case of a concurrent multiband LNA.

Fig. 7(a) shows plots of the NF and ω_T versus collector current for a bipolar transistor using (16a). The contributions of different noise sources to the overall noise factor, F, are shown in Fig. 7(b).

Now we can make a few observations in this common emitter configuration. First, at low frequencies compared to ω_T, NF is dominated by the base shot noise, while at higher frequencies the collector shot noise is the primary noise contributor. Second, for large collector currents, collector shot noise dominates the NF and, therefore, increasing the collector current *deteriorates* the noise factor F in a linear fashion. For smaller collector currents, the effect of base shot noise on the NF increases and the total NF degrades again. Third, a reduction in the collector current will lower the cutoff frequency[9] ω_T and, hence, increases the NF. As can be seen, this is similar to the well-known behavior of a single bipolar transistor amplifier where the $F_{\rm min}$ reaches a minimum for a certain collector current [29].

In the case of MOS transistors, there are more degrees of freedom in the design, such as finger width W_f and the number of fingers n_f. It is clear that the fingers should be as short as the technology allows minimizing r_g for any given overall device width, W. Of course, we can control W by adjusting n_f ($W = W_f \cdot n_f$). A larger W results in a smaller r_g and, hence, a smaller gate-resistance noise contribution. However,

[9]More accurately, ω_T is given by $\omega_T^{-1} = \tau_T = \tau_F + C_{je}/g_m + C_\mu/g_m$

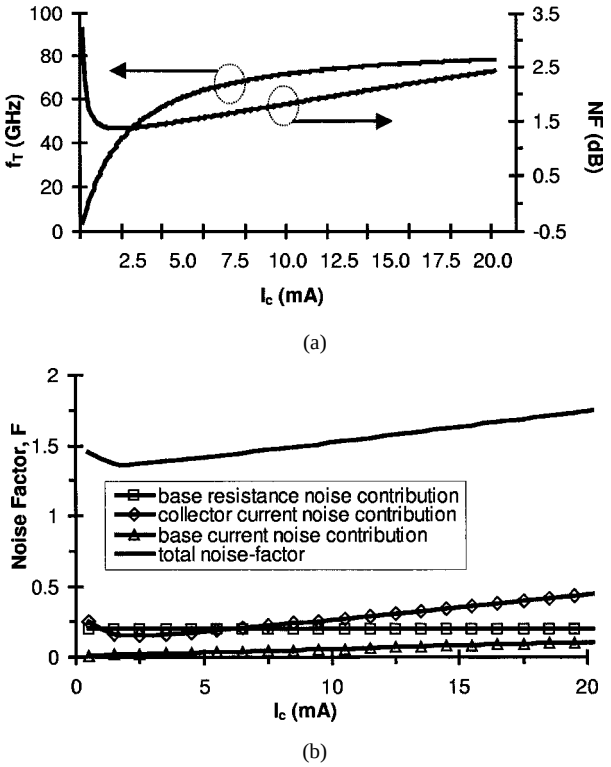

Fig. 7. (a) NF and f_t for a bipolar transistor with $\tau_F = 3.67$ ps. (b) Different noise contributions to the total NF from (16a) (NF numbers for 5.8 GHz).

while a larger W increases the transistor's transconductance g_m, it also increases the drain current consumption and has a negative overall effect on drain noise current contribution to the amplifier's NF. Therefore, there is an optimum W and, hence, an optimum n_f resulting in the lowest NF in this topology (Fig. 8). This approach does not compromise the voltage gain significantly, as it is shown in the next section that the voltage gain of this amplifier is independent of device transconductance and the number of fingers to the first order.

The other parameter of interest is the gate–source overdrive voltage $V_{od} = V_{\rm gs} - V_{\rm th}$ of the MOS transistor. For small values of V_{od}, g_{d0} and g_m increase linearly with V_{od} until velocity saturation occurs and then g_m becomes constant. Meanwhile, g_{d0} and consequently the device noise keep increasing with V_{od}. As can be seen from (16a) and (16b), the drain noise contribution to F is proportional to g_{d0} and inversely proportional to the square of g_m. Therefore, NF drops with V_{od} in the beginning and then rolls back up, as can be seen in Fig. 9(a). It also shows graphs of I_d, g_m and g_{d0} versus V_{od} for the same transistor in a typical 0.18-μm CMOS process. As can be seen from the figure, further increase of V_{od} beyond the optimum NF point will degrade the noise factor and increase the power dissipation. The individual contributions of different noise sources of the same transistor to the total NF are shown in Fig. 9(c).

In practice, passives and substrate resistance noise add to the NF, especially in high-frequency circuits where their relative contributions can be substantial [55]. Also, it is noteworthy that the noise of the equivalent channel resistance $r_{\rm gs}$[10] in series with $C_{\rm gs}$ at high frequencies is already taken into account in the gate-induced noise expressions in (10). Some authors (e.g., [56]) consider the channel resistance noiseless while others (e.g., [25])

[10]It should be noted that this channel resistance is different from $r_{\rm on}$ of MOS transistor in the linear (ohmic) region.

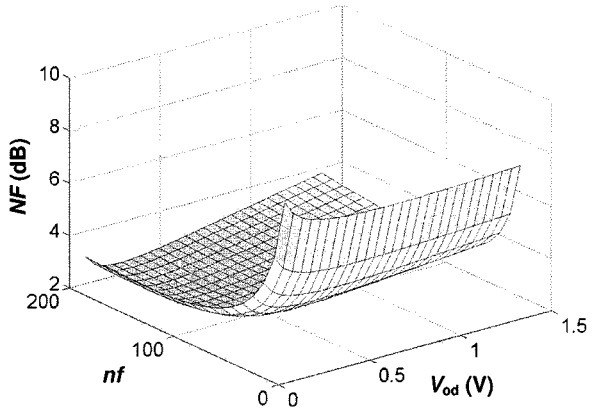

Fig. 8. NF of a 0.18-μm CMOS transistor at 5.8 GHz with finger width of 2 μm versus n_f and V_{od}.

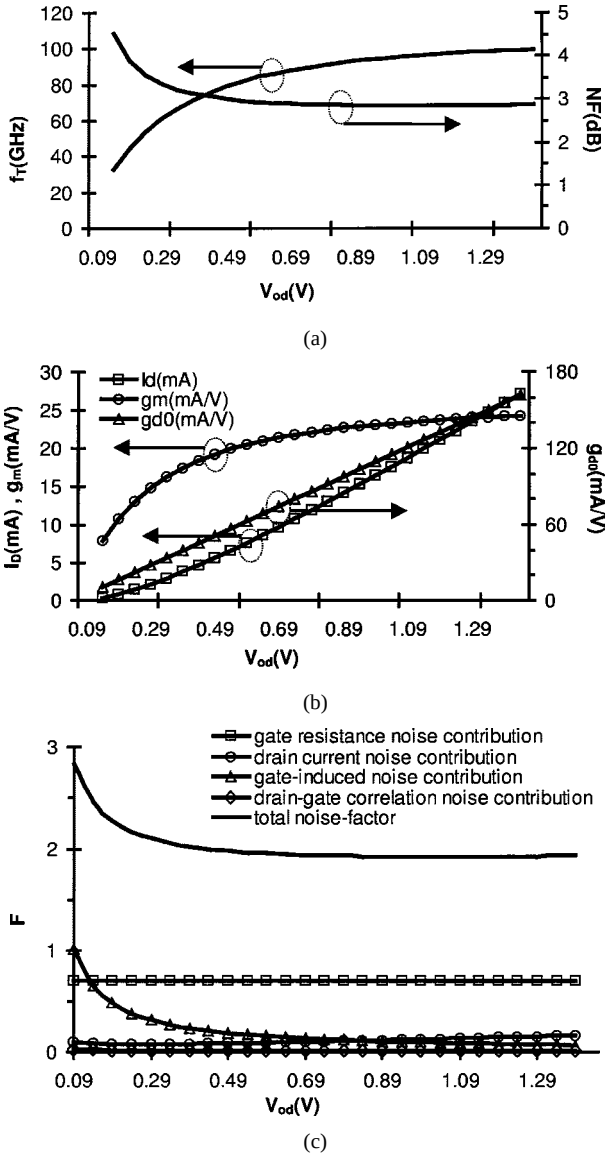

Fig. 9. (a) NF, f_T of a 20 × 2.5 μ/0.18 μ CMOS transistor. (b) I_D, g_m, g_{d0} of the transistor. (c) Different noise contributions to the total NF from (16b) (NF numbers at 5.8 GHz).

modeled it as a noisy resistor. However, it should be noted that channel resistance and gate-induced noise originate from the same distributed gate effect (or nonquasi-static effect) in MOS transistors and the complete noise expressions similar to (10) should be used [50]. Although its noise is already taken into account, channel resistance $r_{\rm gs}$ will affect the expressions for input matching and should be considered in the design process [57], [56].

Once again, we would like to remind the reader that the above discussion is equally valid for concurrent multiband LNAs, as well as single-band implementations, as no explicit assumptions regarding the number of frequency bands have been made.

D. Load Circuit, Output Matching, and Gain

While the input and output of a stand-alone LNA usually need to be matched to 50 Ω to transfer the power efficiently using transmission lines, the output of an LNA in an integrated front-end does not necessarily have to be matched in a similar way. Usually an integrated LNA drives the capacitive input of the first down-conversion mixer in the receiver chain and, hence, it is not desirable to match the output to a real impedance. This difference also explains why it is more common to report some form of power gain (e.g., G_p or S_{21}) for stand-alone LNAs, and the voltage gain Av for the LNAs in integrated front-end circuits. The NF expression for the receiver using voltage gain and input-referred voltage sources can be derived when the output of the LNA is not impedance matched [18].

Assuming no body effect ($g_{mb}=0$) and a small $C_{\rm gd}$ ($Z_{\rm gd}=\infty$), the voltage gain expression of (22) simplifies to

$$|A_v| = \left|\frac{V_{\rm out}}{V_{\rm in}}\right| = \left|\frac{g_m Z_{\rm gs} Z'_L}{Z_{\rm in}}\right| \tag{17}$$

which can be used to calculate the gain at all frequencies. At the frequency bands of interest where (13) holds for minimum NF, (22) further reduces to

$$|A_v| = \left|\frac{Z'_L}{Z'_s + \dfrac{R_{\rm min}}{g_m Z_{\rm gs}}}\right| \approx \left|\frac{Z'_L}{Z_s}\right|. \tag{18}$$

If Z_s is implemented as an inductor to provide the real part of the input impedance, its value is given by (2) which is almost independent of the bias current in a deep velocity-saturated short-channel MOS transistor and also in a bipolar transistor as mentioned in Section IV-B. Therefore, voltage gain given by (18) will be independent of current to the first order. In this case, increasing the bias current will only increase the NF with no significant improvement in A_v.

To achieve the highest gain and selectivity at the frequencies of interest, it is desirable to use a multiresonant load at the output whose impedance is maximum at the frequencies of interest. An example of such load networks will be shown in Section V.

E. Concurrent Multiband LNA Linearity Measures

Linearity is an important measure in the receiver as it determines the size of the largest signal that can be handled by the receiver and controls its dynamic range. The linearity of a single-band LNA is often described using its nth-order intercept point IPn and 1-dB compression point $CP1$. In a concurrent multiband LNA, the $IP3$ and $CP1$ in each band with no significant signal in the other bands are still important and will be referred to as $IP3_{\rm inband}$ and $CP1_{\rm inband}$, respectively. However, due to its concurrent multiband nature, other nonlinearity measures should also be considered. A strong signal in any band can compress the LNA gain at all frequencies. A *cross-band* compression measure can be defined as the signal power in band A that causes a 1-dB drop in the small-signal gain in band B which will be denoted as $CP1_{A>B}$. In addition to this cross-band compression, in-band signals from different desired bands can mix due to the amplifier's nonlinearity and cause in-band undesired signals, as shown in Fig. 10. We show the input intercept point associated with this cross-band intermodulation as $IPn_{\rm crossband}$, where n is the order of nonlinearity leading to this effect.

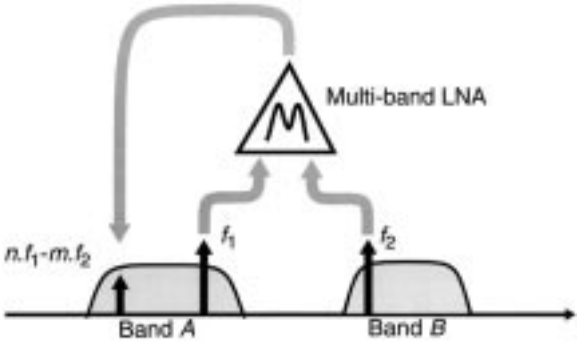

Fig. 10. Illustration of cross-band intermodulation.

We can derive expressions for the nonlinearity measures of concurrent multiband LNAs in terms of device nonlinearity similar to the case of single-band LNAs [60]. We can also relate these cross-band nonlinearity measures to the single-band ones.

Assuming the amplifier output has a third-order polynomial dependence on the input

$$V_{\rm out} = a_1 V_{\rm in} + a_2 V_{\rm in}^2 + a_3 V_{\rm in}^3 \tag{19}$$

we can calculate the in-band and cross-band 1-dB compression points

$$CP1_{\rm inband} = \sqrt{\frac{4}{3}(10^{-0.1}-1)\cdot\frac{a_1}{a_3}} \tag{20a}$$

$$CP1_{\rm crossband} = \sqrt{\frac{2}{3}(10^{-0.1}-1)\cdot\frac{a_1}{a_3}}. \tag{20b}$$

As can be seen from the above equations, the cross-band 1-dB compression occurs 3 dB earlier than the in-band one. This suggests that, for the same amount of nonlinearity, a concurrent multiband LNA needs to be 3 dB more linear than its single-band counterpart. If different applications at various bands have maximum signal powers, the concurrent multiband LNA has to be 3 dB more linear for the strongest signal when compared to a single- band LNA.

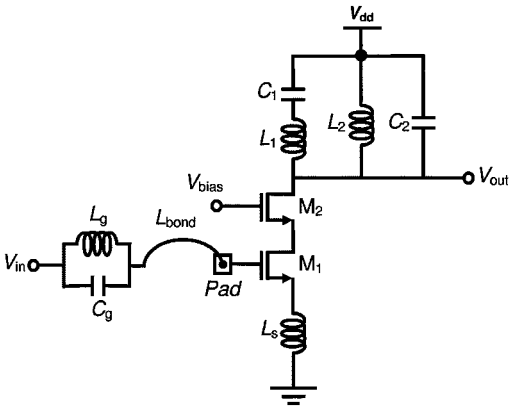

Fig. 11. Concurrent dual-band CMOS LNA (biasing circuitry not shown).

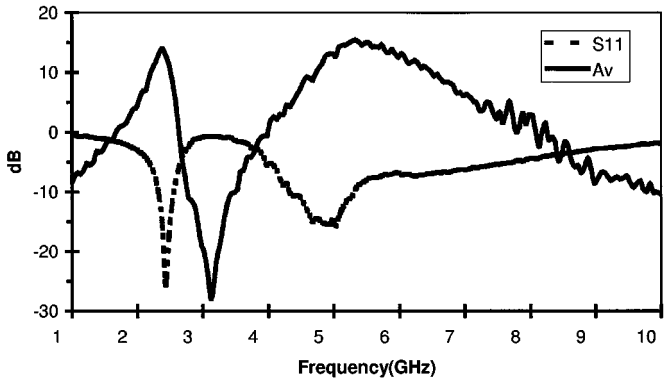

Fig. 12. Measured voltage gain and S_{11} in concurrent dual-band CMOS LNA of Fig. 11.

V. LNA Design Examples and Measurement Results

Having established the theoretical framework for the design of concurrent multiband LNAs, in this section we demonstrate an example of a dual-band concurrent LNA operating at 2.45 and 5.25 GHz. It should be noted that this example shows just one of the many possible implementations following the general treatment of the previous section.

While (21) and (23) provide numerous ways to design the input matching network for any number of frequency bands, we can use the more simplified expressions in (1) and (13) to achieve simultaneous input matching and minimum NF at two frequencies. We note that (2) can also be satisfied for multiple frequencies if $Z_{\rm gs}$ and Z_s are dual circuits, i.e., $Z_{\rm gs}Z_s = k$, where $k = R_{\rm in}/g_m$ is constant. As mentioned earlier, we need to maximize $Z_{\rm gs}$ in order to minimize the NF. One way to obtain a reasonably large $Z_{\rm gs}$ is to use a transistor with minimum channel length and no extra passive elements between the gate and the source. The condition set by (2) can be satisfied using a single on-chip source degeneration inductor similar to the single-band case of [23] and [24]. Since passive components realized on silicon substrate are normally very lossy, having them at the input of the amplifier seriously degrades the NF of the LNA. To fulfill (13) at both frequencies, a parallel *LC* network in series with the inevitable inductance of the bonding wire and package lead is used as shown in Fig. 11. The parallel *LC* network of Z_g is designed to resonate with $Z_{\rm gs}+Z_s$ at both frequency bands of interest.

The drain load network should exhibit high impedance only at frequencies of interest in order to achieve concurrent multiband gain. This requirement can be fulfilled by adding a series *LC* branch in parallel with the parallel *LC* tank of a single-band LNA, as shown in Fig. 11. Each series *LC* branch introduces a zero in the gain transfer function of the LNA at its series resonant frequency that determines the frequency of the notches in the transfer function. This notch is used to enhance the image rejection of the receiver, as discussed in Section III and shown in Fig. 4. Equation (16b) was used to obtain the optimum device size and the dc current.

A concurrent dual-band CMOS LNA implemented in a 0.35-μm BiCMOS technology using only CMOS transistors operates at 2.45 and 5.25 GHz. The input parallel resonator is made using a 0.9-pF porcelain multilayer capacitor and a 2.7-nH chip inductor.

TABLE II
Performance Summary of the Concurrent Dual-Band CMOS LNA

Frequency	2.45 GHz	5.25 GHz
Voltage Gain	14 dB	15.5 dB
S_{11}	-25 dB	-15 dB
NF	2.3 dB	4.5 dB
Input $IP3_{\text{in-band}}$	0.0 dBm	5.6 dBm
Input $CP1_{\text{in-band}}$	-8.5 dBm	-1.5 dBm
Input $CP1_{A>B}$	$CP1_{2.4>5.2}$ = -11.5 dBm	$CP1_{5.2>2.4}$ = -5.7 dBm
Input $IP4_{\text{cross-band}}$	7.5 dBm	
DC Current	4 mA	
Supply Voltage	2.5 V	
Active Device	0.35-µm CMOS transistors	

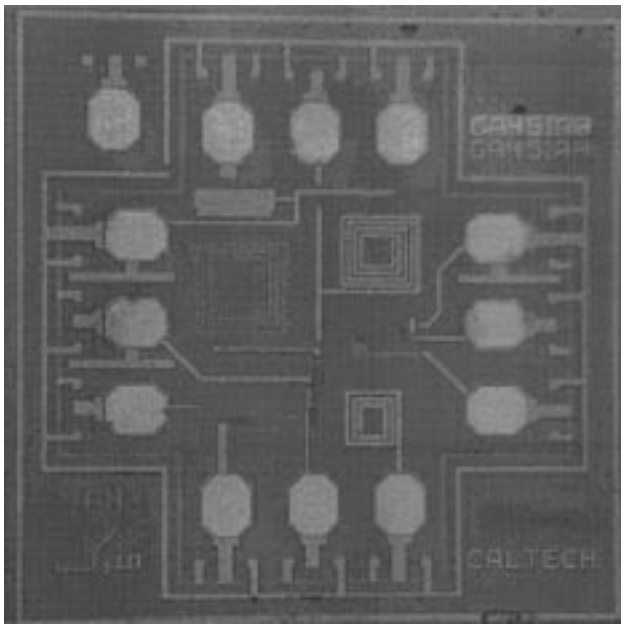

Fig. 13. Chip micrograph for the concurrent dual-band CMOS LNA in Fig. 11.

Fig. 12 shows the measured voltage gain A_v and input reflection coefficient S_{11} of the amplifier up to 10 GHz. The LNA achieves narrow-band voltage gains of 14 and 15.5 dB, input return losses of 25 and 15 dB, and NFs of 2.3 and 4.5 dB at

TABLE III
COMPARISON OF EXISTING SINGLE-BAND CMOS LNAS AND THE CONCURRENT MULTI-BAND LNA AT THE SAME FREQUENCY BANDS (S-BAND AND C-BAND)

Ref.	Tech.	Freq.	NF(dB)	Gain (dB)	S_{11} (dB)	IP_3 (dBm)	CP_{1dB}(dBm)	Power
[62]	0.25-μm PHEMT	5.4GHz	0.76	16	-15	N/A	N/A	N/A
[64]	0.4-μm GaAs	5.2 GHz	1.7	14.5	N/A	-10 (Input)	N/A	3 mA (3 V)
[63]	GaAs HBT	5.7 GHz	2.9	16.2	-7	7 (Output)	21 (Output)	21 mA (3.5 V)
[65]	SiGe HBT	5.8 GHz	1.6	17	N/A	N/A	N/A	7.5 mA (4.5 V)
[66]	0.6-μm CMOS	2.4 GHz	2.3	17.5 (A_v)	-19	1.8 (Input)	-9 (Input)	8 mA (3.3 V)
[59]	0.24-μm CMOS	5 GHz	4.8	18 (A_v)	-12	N/A	N/A	3.6 mA (2 V)
[67]	0.25-μm CMOS	5 GHz	2.5	16 (Gp)	-9.5	N/A	N/A	16 mA (3 V)
This Work [7]	**0.35-μm CMOS**	**2.45 GHz**	**2.3**	**14 (A_v)**	**-25**	**0 (Input)**	**-8.5 (Input)**	**4 mA (2.5 V)**
		5.25 GHz	**4.5**	**15.5 (A_v)**	**-15**	**5.6 (Input)**	**-1.5 (Input)**	

2.45 and 5.25 GHz, respectively. In the course of the NF measurements, special attention was paid to *avoid* methods outlined in [58]. It drains 4 mA of current from a 2.5-V supply voltage. The notch due to the LNA is about 40 dB deeper than the peaks, which directly translates to the same amount of improvement in image rejection. Due to the large difference between the notch and pass-band frequencies, no elaborate tracking loops such as those proposed in [59] are necessary to obtain extra image rejection. The single-ended nature of the LNA makes external Baluns unnecessary. Measurements of six different chips with three different boards and off-chip components show good repeatability without using the sliding capacitor input matching adjustment commonly used in a single-band case [61].

This concurrent dual-band LNA demonstrates input-referred in-band $IP3$s of 0 and 5.6 dBm, and in-band $CP1$s of -8.5 and -1.5 dBm at 2.45- and 5.25-GHz bands, respectively. For this particular frequencies, two tones at 2.50 and 5.15 GHz can combine through the fourth-order nonlinearity to produce an in-band signal at 2.35 GHz (i.e., $4 \times 2.50 - 1 \times 5.15 = 2.35$). The measurements show that this input referred to as $IP4_{\text{crossband}}$ is 7.5 dBm. The LNA exhibits a $CP1_{2.4>5.2}$ of -11.5 dBm and a $CP1_{5.2>2.4}$ of -5.7 dBm. Note the 3-dB difference in in-band and cross-band compression points, as predicted by (20a) and (20b).

Table II summarizes the measured performance of the fabricated concurrent dual-band LNA depicted in Fig. 13. The chip occupies an area of 0.8 mm × 0.8 mm including pads and ESDs.

Table III compares the performance of this concurrent dual-band LNA with previously published single-band LNAs working in one of the same frequency bands. The NF, S_{11}, and power dissipation are comparable or better than previously published nonconcurrent single-band CMOS LNAs.

VI. CONCLUSION

The new concept of a concurrent multiband LNA with the intention of use as the essential part of a concurrent multiband receiver is introduced. One implementation of such a new concurrent dual-band receiver architecture capable of simultaneous operation at two different frequency bands is introduced. It uses a novel concurrent dual-band LNA, combined with an elaborate frequency conversion scheme to reject the out-of-band signals. A general methodology is also provided to achieve simultaneous narrow-band gain and input matching while offering a low NF in concurrent multiband LNAs. The effectiveness of the proposed methodology is demonstrated through measurement results of a CMOS implementation of the integrated concurrent dual-band LNA that achieves a superior NF, S_{11}, and power dissipation over previously published nonconcurrent and/or single-band LNAs.

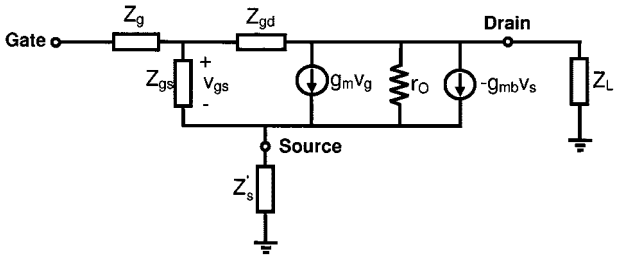

Fig. 14. Simplified small-signal model of Fig. 5 when bulk is ac grounded.

APPENDIX A

Fig. 14 is the equivalent small-signal model for the circuit in Fig. 5 where the bulk is ac-grounded. To simplify this equivalent model, we define $Z_s' = Z_s || Z_{sb}$ and $Z_L' = Z_L || Z_{db}$, where Z_{sb}, Z_{db} are the source–bulk and drain–bulk impedances.

The transistor's output resistor, r_o, can be neglected, because it is relatively large compared to relatively small impedances in an RF circuit. Then, the small-signal input impedance and the voltage gain of this circuit are given by

$$Z_{\text{in}} = Z_g + (Z_L' + Z_{\text{gd}}) \cdot \frac{Z_{\text{gs}} + Z_s'(1 + g_m Z_{\text{gs}})}{Z_{\text{gs}} + [Z_s'(1 + g_{mb} Z_L') + Z_L'] \cdot (1 + g_m Z_{\text{gs}}) + Z_{\text{gd}}} \tag{21}$$

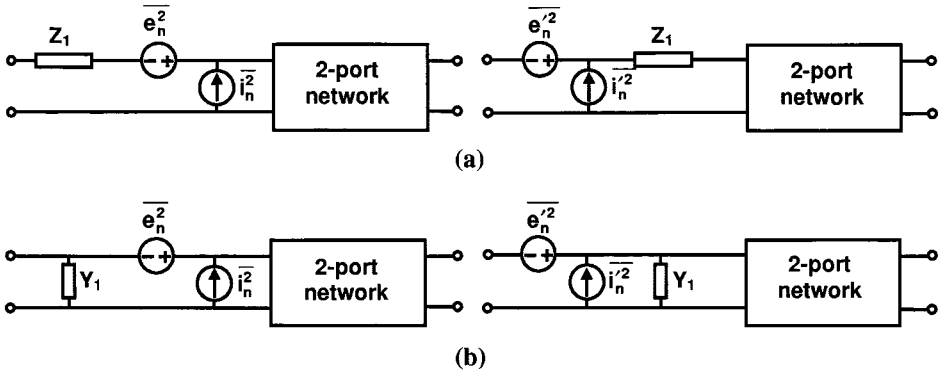

Fig. 15. Effect of adding an impedance to the input of a two-port network on equivalent input noise sources: (a) series impedance and (b) parallel impedance.

$$A_V = \frac{Z_{\rm in} - Z_g}{Z_{\rm in}} \cdot (Z_L' \| Z_{\rm gd}) \cdot \left[\frac{1}{Z_{\rm gd}} - \frac{g_m Z_{\rm gs} - g_{mb} Z_s'}{Z_{\rm gs} + Z_s'[1 + (g_m + g_{mb}) Z_{\rm gs}]} \right]. \quad (22)$$

The input admittance can also be written as the parallel combination of equivalent admittances, i.e.,

$$Y_{\rm in} = \frac{1}{Z_g} \cdot \left\| \left\{ \begin{array}{l} \dfrac{1}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs})} + \dfrac{1}{Z_L' + Z_{\rm gd}} + \dfrac{g_{mb}}{1 + \dfrac{Z_{\rm gd}}{Z_L'}} \\ + \dfrac{1}{1 + \dfrac{Z_{\rm gd}}{Z_L'}} \cdot (g_m - g_{mb}) \cdot \dfrac{Z_{\rm gs}}{Z_{\rm gs} + Z_s'(1 + g_m Z_{\rm gs})} \end{array} \right\}. \quad (23)$$

APPENDIX B

Adding a noiseless[11] one-port network with an impedance Z_1 in series with the input of a given noisy two-port network [see Fig. 15(a)] modifies its input referred equivalent current and voltage sources in the following way:

$$i_n' = i_n$$
$$e_n' = e_n + Z_1 \cdot i_n. \quad (24)$$

Similarly, adding a noiseless one-port network with an admittance Y_1 in parallel with the input of a given noisy two-port network [see Fig. 15(b)] modifies its input referred equivalent current and voltage sources as follows:

$$i_n' = i_n + Y_2 \cdot e_n$$
$$e_n' = e_n. \quad (25)$$

ACKNOWLEDGMENT

The authors would like to thank members of the Caltech High-Speed Integrated Circuits (C.H.I.C.) and Microwave and RF groups, particularly, I. Aoki, H. Wu, L. Chung, and S. Kee for assistance with measurements, and A. Komijani, D. Lu, B. Analui, and M. Morgan for their comments on the manuscript. The authors also thank Conexant Systems, Newport Beach, CA, for chip fabrication, especially R. Magoon, F. Intveld, R. Hlavac, A. Vo, J. Powel, T. Whistler, and S. Lloyd for their support during chip tape-out. The authors also appreciate helpful technical discussions with S. Weinreb, Jet Propulsion Laboratory, Pasadena, CA, H. Samavati, Stanford University, Stanford, CA, and Y. Cheng, Conexant Systems, Newport Beach, CA.

[11]In the case of a noisy Z_1, its equivalent voltage noise source will be simply added to e_n.

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